In Application Serial No. 10/805,158
Filed May 19, 2004

DECLARATION OF DAVID R. EVANS UNDER 37 CFR §1.132

I, David Russell Evans, Ph.D., hereby declare as follows:

1. My residence address is 7574 S.W. 179th Street, Beaverton, Oregon 97007.

2. Since April 1, 1999 I have been employed by Sharp Laboratories of America, Inc. ("SLA"), 5700 N.W. Pacific Rim Boulevard, Camas, Washington 98607, and between 1993 and April 1, 1999 I was employed by SLA's predecessor company, Sharp Microelectronics Technology, Inc. ("SMT"), located at the same address. My titles at SMT (until April 1, 1999) were, originally, Principal Engineer and, later, Senior Member of the Technical Staff, and my title at SLA, since April 1, 1999, is Senior Manager. My responsibilities include developing advanced process technologies to improve microelectronics fabrication. My technical experience is detailed in the accompanying CV.

3. I have read the claims for the patent application in question, Ono et al., Serial Number 10/805,158 (the Applicant), entitled "Charge Trap Non-Volatile Memory Structure for 2 Bits per Transistor". I have read the Office Action dated March 10, 2006, where claims 16, 17, 20-22, and 25-27 have been rejected as obvious by Halliyal (US 6,451,641), in view of King (US 6,754,104) and Kirkpatrick (US 4,197,144). I have also reviewed the Chooi (US 6,486,080), Agarwal (US 2001/0015453), Liang (US 5,372,957), and Moslehi (US 5,846,883) references cited by the Examiner.

4. The Examiner, on page 4, claims that Halliyal describes all the steps of claim 16, except for the step of inducing trapping centers in a dielectric material. The Examiner further claims that it would have been obvious to one of ordinary skill in the art to induce trapping centers into the dielectric material by exposing the dielectric to an ionized species, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer.

5. As explained in the Applicant's specification (pages 1-3), there exist two fundamental non-volatile memory device types: they are floating gate and NROM devices. The floating gate design uses a conductive charge trapping layer, and is not especially relevant to this discussion. The NROM design uses an oxide/nitride/oxide (ONO) structure, interposed between a gate electrode and a FET channel region, where the nitride layer is a non-conductive charge trapping layer. The tradeoff between oxide quality and oxide thickness has encouraged some manufacturers to replace the ONO oxide layers with high-k insulating materials. The Applicant's invention simplifies the problem by replacing the entire ONO structure with a single (non-conductive) high-k dielectric charge trapping layer. Insulating layers are not needed between the Applicant's charge trapping channel and the channel. Neither is an insulator needed between the charge trapping layer and the gate electrode.

6. Halliyal describes a conventional FET made with a high-k dielectric. Halliyal does not describe charge trapping, or the use of a FET as a memory. Halliyal's high-k dielectric cannot store a charge. Halliyal is concerned with depositing polysilicon or silicon-germanium in a manner that does not damage a high-k dielectric. I see no correlation between the Applicant's memory device and Halliyal's FET process.

7. King describes a number of different embodiments that use the combination of a depletion-mode insulated-gate FET (IGFET) and a negative differential resistance (NDR) FET. An IGFET is a conventional FET device. In column 14, King describes the formation of a first electrical insulating layer 1020, with charge traps at or near the interface to the Si substrate 1000. A second (gate) insulator layer 1040 is formed over the first insulator layer 1020, and King describes techniques for forming charge traps in the gate oxide layer (column 14, line 55 through column 15, line 14).

While King does describe the formation of charge traps in an insulator material, such as a high-k dielectric, it is important to understand that these charge trap regions have nothing to do with non-volatility. Rather, King uses his charge traps to create a negative differential resistance (NDR). I see no crossover between NDR and non-volatile memory applications.

8. Kirkpatrick describes a PIN diode device that can be used as a memory because of charge traps formed in the insulator (I) between the PN junction. The insulator is SiO2, and the trapping sites are formed by implanting Si ions.

9. The Examiner's rationale for combining these three references is not clear to me. Of the three references, only one reference (Kirkpatrick) describes a memory device. Unlike the Applicant's invention, Kirkpatrick describes a diode active device with trapping centers in the SiO2 insulator between the P and N regions. The Applicant does not describe a SiO2 insulator, an insulator between P and N regions, or a diode active device. It appears to me that the Examiner could not have found a memory device that is more different from the Applicant's device than Kirkpatrick's.

Of the three primary prior art references presented by the Examiner, the Halliyal and King references seem even more distant from the Applicant's. While the King and Halliyal devices both use a high-k dielectric, neither of these devices can be used for a non-volatile memory. While King describes a high-k dielectric gate oxide with charge trapping centers, King's charge trapping centers cannot hold a charge or store a memory state.

In summary, I can find no apparent reason for an expert in the art to combine three such disparate references as the King, Halliyal, and Kirkpatrick references. Further, I can unequivocally state that this combination does not suggest a memory transistor invention. Even further, the combination of references does not suggest a memory transistor that is able to replace the conventional ONO structure with the high-k dielectric charge trapping region described by the Applicant.

10. In reviewing the other rejections made in view of the Chooi, Agarwal, Liang, and Moslehi references, I note that even if it would have been obvious to add the features cited in these supplemental references, the combination of any or all of these references with Halliyal/King/Kirkpatrick still fails to suggest a device with all the features described in Applicant's claim 16. For example, with respect to claim 28, even if it would have been obvious to use Moslehi's ICP source in combination with Halliyal/King/Kirkpatrick, that combination would not suggest a non-volatile memory transistor made with a high-k gate dielectric, without underlying or overlying oxide layers, where charge trapping centers are formed in the high-k dielectric. Likewise, the

addition of Liang's angled implantation, or Chooi/Agarwal's densification annealing, even when combined with Halliyal/King/Kirkpatrick, does not describe the features of Applicant's claim 16. Therefore, I do not consider these supplemental references particular relevant to the issue of whether the Applicant's invention is obvious.

11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

31 July 2006
Date

David R. Evans

David Russell Evans

Professional Education:

1981 Ph. D. in Physical Chemistry, Iowa State University, Ames, Iowa. Dissertation: "A Comparative Study of Classical and Quantal Approaches to Thermal and Diffusive Transport in a Dilute Atom-Diatom Binary Mixture"

1974 B. S. in Chemistry, Summa Cum Laude, (GPA 3.98) University of Missouri-Rolla, Rolla, Missouri.

Employment History:

5/1999 - Present

Sr. Manager, Dept. 5, SHARP Laboratories of America, Inc.

Responsible for project management and technical guidance of advanced resistive memory project. Previously, directed CVD copper interconnect research and development. In addition, manage chemical synthesis and associated material development. Directly responsible for advanced CMP research directed toward novel device structures, advanced perovskite materials, noble metals, nanostructures, and sensors.

5/1994 – 5/1999

Sr. Member of Technical Staff, Process Technology Laboratory, SHARP Microelectronics Technology, Inc.

Major responsibility was research and development of chemical mechanical polishing (CMP) of copper for advanced interconnect and dielectric materials for shallow trench isolation and related device structures.

11/1988 - 5/1994

Principal Engineer, Integrated Circuit Operations, Tektronix, Inc.

Major responsibility was thin film development and manufacturing, primarily for use as diffusion barriers and thin film resistors.

11/1986 - 11/1988

Principal Engineer, Liquid Crystal Strategic Program Unit, Tektronix, Inc.

Major responsibility was large area photolithography for optical shutters and passive matrix flat panel displays.

10/1980 - 11/1986

Sr. Development Engineer, Bipolar Process Development Dept., Tektronix, Inc.

Major responsibility was plasma etching and deposition. Implemented the first plasma etch processes for integrated circuit fabrication in Tektronix.

Teaching Experience:

9/1994 – 10/2004

Adjunct Faculty-Oregon Graduate Institute of Oregon Health and Science University

Graduate level course, Microelectronics Fabrication I, ECE 560, during fall term: The course covers semiconductor materials, crystal structure and growth, thermal oxidation, ion implantation and diffusion. It is part of a one-year sequence in semiconductor processing that typically is taken both by matriculating graduate students from and working professionals drawn from local industry.

3/1981 – 5/1981

Instructor-Iowa State University

Undergraduate level course, Physical Chemistry: The course covered chemical reaction kinetics, kinetic theory of gases, transport theory, x-ray diffraction and crystal structure. Prepared all lectures and exams.

Refereed Journal and Proceedings Publications:

David R. Evans and Michael R. Oliver, Chemical Mechanical Planarization-Integration, Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 189, 2005 (invited). "Abrasive Contribution to CMP Friction"

Parshuram B. Zantye, S. Mudhivarthi, Ashok Kumar, and David Evans, , Chemical Mechanical Planarization-Integration, Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 75, 2005. "In-situ Metrology for End Point Detection during Chemical Mechanical Polishing of Shallow Trench Isolation Structure"

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David R. Evans, Michael R. Oliver, and Mike Kulus, Chemical Mechanical Planarization IV, Electrochem. Soc. PV-2000-26, Pennington, NJ, pg. 122, 2001. "Morphology Evolution during Copper CMP: Comparison of Fixed Abrasive and Conventional Pads"

Weiwei Zhuang, Lawrence J. Charneski, David R. Evans, and Sheng Teng Hsu, Advanced Metallization Conference 1999, Mater. Res. Soc., Warrendale, PA, pg. 213, 2000. "New Copper Precursor for Chemical Vapor Deposition of Pure Copper Thin Films"

Y. Ma, D. R. Evans, T. Nguyen, Y. Ono, and S. T. Hsu, *IEEE Elec. Dev. Lett.*, 20(5), 254, 1999. "Fabrication and Characterization of Sub-Quarter-Micron MOSFET's with a Copper Gate Electrode"

Yanjun Ma, Douglas J. Tweet, Larry Charneski, and David R. Evans, Advanced Metallization Conference in 1998, Mater. Res. Soc., Warrendale, PA, pg. 357, 1999. "Density Oscillation in Sputtered Tantalum Nitride Barrier Metal Thin Films"

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D. R. Evans, Chemical Mechanical Planarization I, Electrochem. Soc. PV-96-22, Pennington, NJ, pg. 70, 1997. "Electrochemical Interaction between Copper and Barrier Materials During Chemical Mechanical Polishing"

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Z. Karim and D. Evans, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 101, 1996. "Improvement of the Dielectric Properties of Silsesquioxane Based Spin-on-Polymer by Plasma Treatment and Other Novel Techniques"

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G. T. Evans and D. R. Evans, *J. of Chem. Phys.*, 81(12), 6039, 1984. "Kinetic Theory of Rotational Relaxation in Liquids: Smooth Spherocylinders and Rough Sphere Models"

D. R. Evans, Plasma Processing IV, Electrochem. Soc. PV-83-10, Pennington, NJ, pg. 199, 1983. "Dry Etched Vias for Two Layer Interconnect on High Density Bipolar Integrated Circuits"

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Yanjun Ma, Yoshi Ono, Lisa Stecker, David R. Evans, and S. T. Hsu, *IEEE Int. Elec. Dev. Mtg. 1999*, Washington, DC, Dec. 5-8, 1999. "Zirconium Oxide Based Gate Dielectrics with Equivalent Oxide Thickness of Less Than 1.0 nm and Performance of Submicron MOSFET using a Nitride Gate Replacement Process"

David Evans, Bruce Ulrich, Michael Oliver, and Sharath Hosali, *1999 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 8-11, 1999. "Polysilicon Polish Stop for STI CMP Using Experimental Slurry"

David J. Stein, Dale L. Hetherington, James E. Stevens, Michael R. Oliver, Sharath D. Hosali, and David R. Evans, *1999 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 8-11, 1999. "Oxide CMP Using Ceria-based Slurries"

S. T. Hsu, D. Evans, T. Nguyen, and H. Yang, *Sixth Symp. on Nano Device Technology*, National Nano Device Laboratories, National Science Council, Taiwan, ROC, May 12-13, 1999. "Cu/a-F:C Interconnect Technology"

D. R. Evans, *1999 Int. Conf. On GaAs Manufacturing Technology*, Vancouver, BC, Canada, Apr. 19, 1999 (invited). "The Role of CMP in the Fabrication of Advanced Interconnect"

H. Yang, D. R. Evans, T. Nguyen, L. Stecker, B. Ulrich, and S. T. Hsu, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Multilevel Damascene Interconnection in Integration of MOCVD Cu and Low-κ Fluorinated Amorphous Carbon"

David J. Stein, Dale L. Hetherington, James E. Stevens, Michael R. Oliver, Sharath D. Hosali, and David R. Evans, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Investigation of a Self-stopping ILD CMP System"

H. Yang, D. R. Evans, T. Nguyen, L. Stecker, B. Ulrich, and S. T. Hsu, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Multilevel Damascene Interconnection in Integration of MOCVD Cu and Low-κ Fluorinated Amorphous Carbon"

Tue Nguyen, Hongning Yang, David Evans, Bruce Ulrich, Lisa Stecker, and Sheng Teng Hsu, *1998 Advanced Metallization Conf.*, Colorado Springs, CO, Oct. 6-8, 1998. "Integration of MOCVD Copper and Low-κ Fluorinated Amorphous Carbon in Single and Dual Damascene Interconnection"

David Evans, *CMP Technology for ULSI Interconnection Seminar at SEMICON West*, San Francisco, CA, Jul. 14, 1998 (invited). "Pattern Dependence and Planarization for Shallow Trench Isolation"

T. Nguyen, H. Yang, D. R. Evans, and S. T. Hsu, *1998 VLSI Multilevel Interconnection Conf. (VMIC)*, Santa Clara, CA, Jun. 16-18, 1998, pg. 31. "Integration of MOCVD Copper and Low-κ Fluorinated Amorphous Carbon in Single Damascene Structures"

H. Yang, D. Evans, J. Takason and T. Hara, *ECS Meeting-Spring 1998*, San Diego, CA, May 5, 1998 "Thermal Stability of Organic Interlayers with Low Dielectric Constant"

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Tue Nguyen, Dave Evans, and Sheng Teng Hsu, *1997 VLSI Multilevel Interconnection Conf. (VMIC)*, Santa Clara, CA, Jun. 10-12, 1997. "Integration of MOCVD Copper Metallization with SIMOX Devices"

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Continuing Education and Other Skills:

Broad experience related to collaborative research and development efforts with universities, government laboratories, and private companies. This includes writing legally binding contracts and statements of work, administering grants, and managing collaborative efforts of a more informal nature.

Taken several electrical engineering courses through Oregon State University, Portland State University, and University of Portland that cover fundamental circuits and devices. Additionally, have participated in several work-related technical and management training programs.

Proficient in applied mathematics and algorithm construction.